Appendix F

Supplemental Performance Demonstration Information

Appendix F includes:

F.1 Test panel artwork

F.2 Lamination Specifications for DfE Performance Demonstration Panels

F.3 Process Steps for Manufacturing and Drilling DfE Performance Demonstration Panels

F.4 Design for the Environment Printed Wiring Board Project Performance Demonstration Workplan

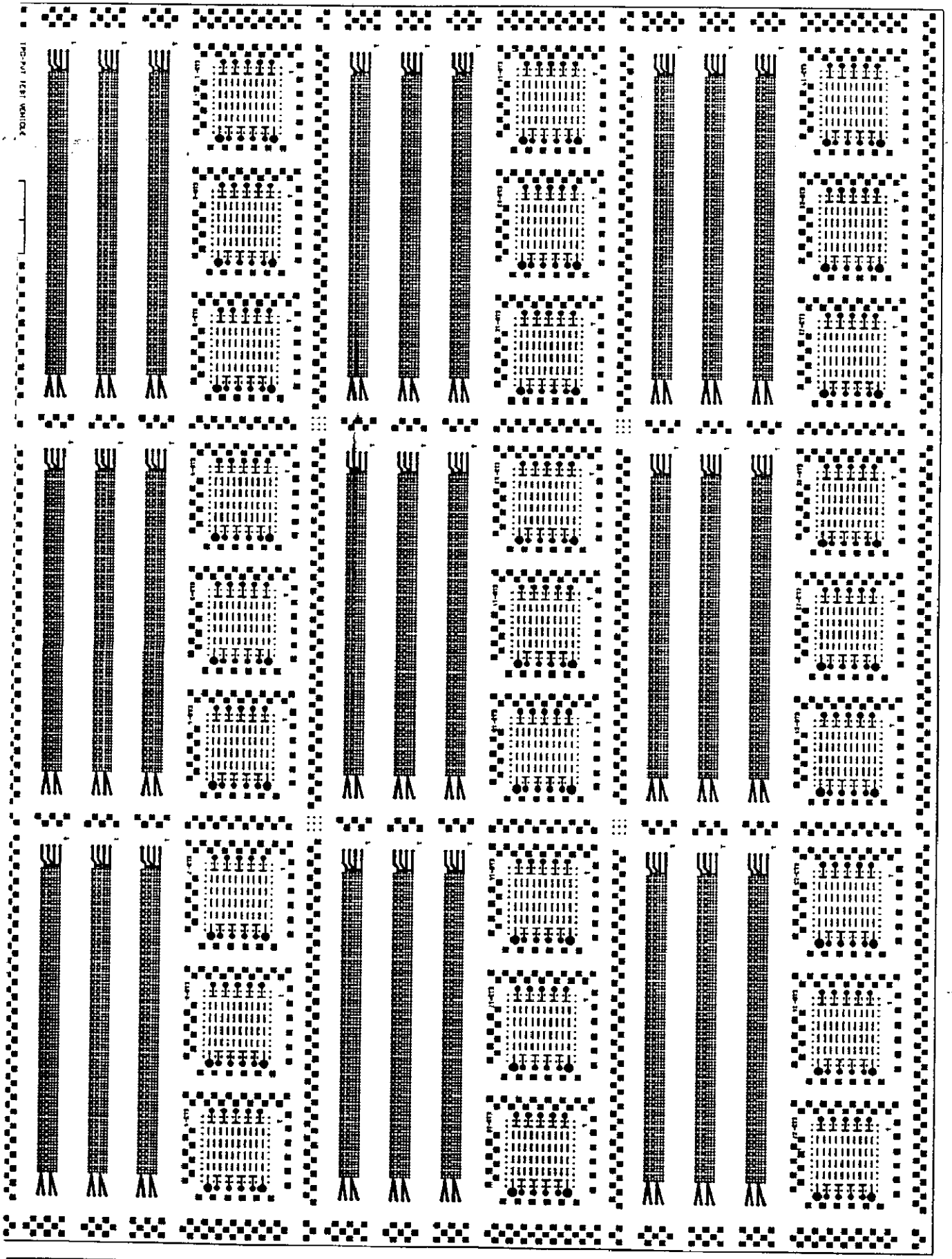
F.5 Process Steps for Electroplating, Etching, HASL, and IR Reflow of DfE Performance Demonstration

F.6 Specifications for IR Reflow of DfE Performance Demonstration Panels

F.7 IPC-TM-650 Test Methods Manual

F.8 IPC TM 650: Protocol for Thermal Stress Test for Plated Through Holes, Number 2.6.8

F.1 Test Panel Artwork



F.2 Lamination Specifications for DfE Performance Demonstration Panels

Layer	Core	Item Description	Copper oz	Material Thickness	Qty Per.
1		Copper Foil 0.5		0.0007	1
		Prepreg 1080		0.0026	2
2/3	1	Standard Core .006	1/1	0.0060	1
		Prepreg 7628		0.0066	2
4/5	2	Standard Core .006	1/1	0.0060	1
		Prepreg 7628		0.0066	2
6/7	3	Standard Core .006	1/1	0.0060	1
		Prepreg 1080		0.0026	2
8		Copper Foil 0.5		0.0007	1
Total Thickness				0.0562	

Board Type: 8 layer multilayer

Board Technology: Through-hole

Board Dimensions: 15.587" x 20.758"

Material Grade: FR-4

Panel Size: 18" x 24"

Line Width: 0.0200

Spacing: 0.0140

Overall Calculated Press Thickness: 0.062 +/- 0.009

F.3 Process Steps for Manufacturing and Drilling DfE Performance Demonstration Panels

1. Clean
2. Laminate dry film
3. Over layers
4. Image
5. Develop
6. Etch/Strip
7. Optical inspect
8. Mechanical inspect
9. Black oxide
10. Converter
11. Bake @250° C for one hour
12. Lay-up/press
13. Drill
14. Final inspection
15. Put panels in bags with desiccant
16. Ship panels to individual MHC test sites

F.4 Design for the Environment Printed Wiring Board Project Performance Demonstration Methodology

Note: This workplan provides the general protocol for the Design for the Environment (DfE) Printed Wiring Board (PWB) Project Performance Demonstration, which will generate information for the PWB Cleaner Technologies Substitutes Assessment (CTSA) on the "making holes conductive" step of the PWB manufacturing process. The workplan is based on input from representatives of the PWB industry, industry suppliers, EPA, the University of Tennessee Center for Clean Products and Clean Technologies, and other stakeholders of the DfE PWB Project. There may be slight modifications to the workplan as preparations for the performance demonstration progress.

I. OVERVIEW

A. Goals

The overall goal of this performance demonstration is to obtain specific information about alternative technologies that effectively make holes conductive. Specifically, the goals are the following: 1) to encourage PWB manufacturers to experiment with new products and workpractices that may reduce environmental and human health risk and result in pollution prevention; 2) to standardize existing information about commonly used technologies; and 3) to gain information about technologies not in widespread use, emerging technologies, or technologies that may be applicable to making holes conductive.

B. General Performance Demonstration Plan

The general plan for the performance demonstration is to collect information about alternative technologies at sites where the technologies are already being used. These sites may be customer production facilities, customer testing facilities (beta sites), or supplier testing facilities, in that order of preference. The test vehicle will be a standardized 8-layer multilayer board that has been used by industry to evaluate accelerated board testing methods. Every attempt will be made to limit the variability associated with the boards that is not due to differences in the technologies being tested. The boards will be produced specifically for this performance demonstration. Information will be collected from each demonstration site during the testing.

C. Characteristics of Alternative Technologies to be Reported from Performance Testing

1. Product cost: Cost per square foot of panel processed. This number will be based on information provided by product suppliers, such as purchase price, recommended bath life and treatment/disposal methods, and estimated chemical and equipment costs per square foot panel per day. "Real world" information from PWB manufacturers, such as actual dumping frequencies, treatment/disposal methods, and chemical and equipment costs will be included. The product cost may differ for different shop throughput categories.

2. Product constraints: Types of board shop processes with which the product is compatible. This information will be submitted by the manufacturers and may also be identified as a result of the performance testing.

3. Special storage, safety and disposal requirements: Flammability or volatility of the product, VOCs, TTOs, HAPS, Prop. 65 chemicals. This information will be requested from the manufacturers and will vary according to the chemicals comprising the products. Manufacturers will provide recommendations on disposal or treatment of wastes associated with the use of their products. The storage and disposal costs will be a factor in determining the adjusted cost of the product.

4. Ease of use: Physical effort required to effectively use the product line, convenience. This is a subjective, qualitative measurement based on the judgment of the product user. Specific questions such as the following will be asked: How many hours of training are required to use this product? What process parameters are needed to ensure good performance? What are the ranges of those parameters and is there much flexibility in the process steps?

5. Duration of production cycle: The measured time of the "making holes conductive" process, number of operators. This information will be used to measure the labor costs associated with the use of the products. Labor costs will be based on the time required for making holes conductive with the specific products and at a standard worker wage. The product cycle has been defined as the desmear step through a flash up to 0.1 mil (includes desmear and flash).

6. Effectiveness of technology, product quality: These characteristics will be assessed based on performance standard measurements such as aspect ratio plated, solder float test, thermal cycling, yield, and CpK (process capability).

7. Energy and natural resource data: This information will be used to measure energy consumption and the variability of energy consumption for the use of different technologies. Measurements of duty and load, for example, will be collected. The information will also address materials use rates and how the rates vary with alternative processes.

8. Exposure data: These data will be used to characterize exposures associated with technologies not in widespread use. Exposure information for more commonly used technologies will be collected in the Workplace Practices Survey, conducted separately from this study.

II. PERFORMANCE DEMONSTRATION PROTOCOL

A. Technologies to be Tested

1. Electroless copper
2. Carbon
3. Graphite
4. Palladium
5. Non-formaldehyde electroless
6. Conductive polymer
7. Conductive ink

B. Step One: Identification of Suppliers and Test Sites/Facilities

Workgroup members will identify any additional suppliers of the above product lines and participate actively in soliciting supplier participation in the performance demonstration. Any supplier that wishes to participate will be eligible to submit their technology, provided that they agree to comply with the testing protocol and submit the requested information.

Suppliers will identify sites that are using their product lines/technologies to make holes conductive according to the priority sites listed below.

First preference for testing sites: customer production facilities
Second preference for testing sites: beta sites - customer testing facilities
Third preference for testing sites: supplier testing facilities

Every vendor is guaranteed testing at one site; a submission of a second site will be subject to the review of the performance demonstration workgroup. The workgroup will decide how many submissions are feasible based on time and resource constraints. If a supplier has more than one substantially different product line, it may submit names of test facilities for each of the product lines.

C. Step Two: Test Vehicle Production and Characteristics

In order to minimize the variables associated with panel production, one manufacturer will produce all of the panels. The time and materials to produce the panels will be donated to the project by industry members. The manufacturer will produce enough 18" x 24" 8-layer multilayer panels to send three panels to each test facility. The artwork and detailed characteristics for the panels are being developed separately in IPC's electroless/electrolytic plating subcommittee. Detailed construction information, when available, will be attached to the performance demonstration workplan. The panels will have the following characteristics:

Material: FR 4 Fiberglass Resin
Laminate thickness: .062 inches
Hole sizes: multiple holes of sizes .013, .018, and .036 inches

The boards will be manufactured at a single shop, stopping before the desmear step. Three panels will be shipped to each test facility to be run through the making holes conductive line, which begins with the desmear step.

D. Step Three: Making Holes Conductive

The panels, once distributed to testing facilities, will be run through the making holes conductive (MHC) process line in operation at the facility. The usual process operator will operate the line in order to minimize error due to unfamiliarity with the technology. The panels will all be processed in the same production run. In order to ensure compatibility with desmear processes, the panels will be desmeared and run through the MHC line at the individual facilities.

Panels that are manufactured with the pattern plate process will be treated slightly differently than panels manufactured with the panel plate process. Panels manufactured with the pattern plate process will first go through the MHC line. Dry film will be applied, and the panels will be developed to remove all resist. The panels will then be flash plated up to 0.1 mil.

Panels that are panel plated will first go through the MHC line, and then be directly flash plated up to 0.1 mil. This process was designed to ensure that resist residues don't interfere with the through-hole plating process. (Note: the process was not meant to test the adhesion of the resist to the panel or to test resist compatibility with different processes.)

After the holes have been flashed to 0.1 mil of electroplated copper, the individual test facilities will ship all of the panels to a single plating facility, where the panels will be electroplated. This procedure will minimize variability due to variation in electroplating techniques.

E. Step Four: Information Collection at Demonstration Facilities

An independent observer will be present when the panels are run through MHC product lines at demonstration facilities. The observer will record information on an Observer Data Collection Sheet during the test. The information requested on this data collection sheet will be discussed with the operator prior to the test.

F. Step Five: Electroplating and Testing of the Boards

After the panels have been completed (holes made conductive and flashed up to 0.1 mil) at the different testing sites, they will be collected at one facility, where they will be electroplated to a thickness of 1 mil. Once finished, the boards will be electrically tested using Interconnect Stress Test (IST) methodology. In addition, they will be microsectioned, and tests such as solder shock and thermal cycling will be conducted.

III. PERFORMANCE DEMONSTRATION PARTICIPANT REQUIREMENTS

A. From the Facilities/Process Operators:

1. Facility will make their process line/process operators available to run three panels in the designated performance demonstration time frame.

2. The process operator will meet with the independent observer briefly before running the first panel through the line to familiarize him/her with the unique aspects of the line. The process operator will be available to assist the independent observer in collecting information about the line when the panels are run through it.

B. From the Vendors/Suppliers of the Process Line Alternatives:

1. Vendors will identify demonstration sites.

2. Vendors will submit product data sheets, on which they will provide information on product constraints, recommended disposal/ treatment, product formulations, etc. The requested information will be agreed upon prior to testing.

F.5 Process Steps for Electroplating, Etching, HASL, and IR Reflow of DfE Performance Demonstration Panels

1. Drill to create tooling holes
2. Apply plating resist (organic photopolymer) - image and develop
3. Electroplate copper
4. Apply etch resist (tin)
5. Strip plating resist
6. Etch
7. Strip etch resist
8. Solder mask - image and develop
9. Hot air solder leveling (HASL)
10. Rout out AT&T B coupons, place in numbered bags
11. Send AT&T B coupons to Robisan Laboratory Inc.
12. Send panels to simulated assembly process (IR Reflow)
13. IR Reflow
14. Package and ship panels to DEC Canada for electrical testing

F.6 Specifications for IR Reflow of DfE Performance Demonstration Panels

The panels containing only IST coupons were processed through a surface mount technology (SMT) oven with the following specifications:

Oven Model	BTU VIP98 Unit
Oven Profile (top and bottom)	Zone 1 = 200 C Zone 2 = 180 C Zone 3 = 170 C Zone 4 = 180 C Zone 5 = 190 C Zone 6 = 240 C Zone 7 = 240 C
Processing Speed	30 inches/minute
Panel Orientation	#1 edge up and leading; shorter (18") edge leading
Panel Spacing	24 inches or 48 seconds
Oven Passes	Two - first 12/29/95 1540 to 1745 second 12/30/95 0801 to 1015
Oven Carrying Support	Wire conveyor
Cooling Between Passes	Horizontally in metal rack, room temperature

*Note: Only IST coupons were processed through IR Reflow

F.7 IPC-TM-650 Test Methods Manual

The Institute for Interconnecting and Packaging Electronic Circuits
2215 Sanders Road Northbrook IL 60062-6135

IPC-TM-650
Test Methods Manual

1.0 Scope This test measures increases in resistance of plated-through hole barrels and inner layer connections as holes are subjected to thermal cycling. Thermal cycling is produced by the application of a current through a specific coupon configuration. In this technique, a chain of plated-through copper barrels and inner layer interconnects are resistance heated by passing DC current through the post interconnect for 3 minutes to bring the temperature of the copper to a designated temperature (slightly above the Tg of the laminate in the sample). Switching the current on and off creates thermal cycles between room temperature and the designated temperature within the sample. This thermal cycling induces cyclic fatigue strain in the plated-through hole barrels and inner layer interconnects and precipitates any infant mortality or latent defects.

The number of cycles achieved permits a quantitative assessment of the performance of the entire interconnect. Correlation has been achieved between IST, Thermal Ovens, Liquid to Liquid Thermal Shock and Thermal Stress (Solder Float) Testing.

Detailed information regarding the test is found in the NOTES 6.0 section.

2.0 Applicable Documents

2.1 IPC-TM-650, Method 2.1.1

2.2 IPC-TM-650, Method 2.1.1.2

3.0 Test Specimens Daisy chain test coupon. For artwork, see Appendix 1. See note 6.1, “Test Coupon.”

4.0 Apparatus or Material

4.1 Interconnect Stress Test System

4.2 Two (2) Four pin, 2.54 mm (0.1 inch) pitch male connectors (MOLEX 2241-4042 or equivalent)

4.3 Sn60Pb40 or Sn63Pb37 Solder

Number 2.6.X	
Subject **Interconnect Stress Technology (IST)**	
Date **6/96**	Revision **Proposal**
Originating Committee: Test Methods Subcommittee (7-11)	

4.4 Solder Flux

4.5 Soldering Iron

4.6 Multimeter - optional

4.7 Microsectioning equipment - optional

5.0 Procedure

5.1 Sample preparation

5.1.1 Solder two 4 pin male connectors to 0.040 inch holes at left and right edges of side 1.

5.1.2 Allow coupons to come to room temperature (minimum 10 minutes), prior to installation onto IST system.

5.2 IST Procedure

5.2.1 Position coupons at each test head by attaching male to female connectors.

5.2.2 Provide system software with specific test conditions. The available ranges and standard conditions are as follows:

Conditions	IST Range	Standard
No. of samples	1-6	6
Test Temp	50°C to 250°C (122°F to 422°F)	150°C (GF) (302°F)
Max. Res. Chng	1-100%	10%
Max No. Cycles	1-1000	250 (1 day)
Data Coll. Freq.	1-100 cycles	10 cycles
Cooling Ratio	0.5-2X heat time	1:1
Table Selection	system/custom	system

5.2.3 Enter a file name and begin test. The IST system continuously monitors the coupons and records the relative changes in resistance of both the barrel and the inner layer connections. Data is compiled to create graphs of each coupon's performance throughout IST stress testing.

5.3 Microsection Evaluation - Optional If detailed failure analysis is desired to determine exact location of separations and/or cracks, microsection of failed coupons shall be performed in accordance with IPC-TM-650, Method 2.1.1 or 2.1.1.2.

6.0 Notes

6.1 Test Coupon. Certain design rules must be applied to achieve thermal uniformity. Electronic design files for coupon construction are available from the IPC office. The coupon resistance should measure between 150 milliohms and 1.5 ohms when measured at room temperature. Two resistance values (voltage drops) for each coupon are monitored independently, using a four wire measurement technique.

The test coupons are incorporated as part of each panel produced to monitor production or can be step and repeated over a single panel and used to develop processes or process change.

6.2 Instrument Details.

6.2.1 Overview of General Steps of Procedure.

6.2.1.1 Data Entry. Identify and enter the specific test conditions.

6.2.1.2 Pre-cycling. The application of a trial DC current to each coupon, that elevates the individual coupons to a predetermined resistance level, relative to the specific resistance (temperature) required for stress testing. Compensations are applied by the equipment until all coupons achieve their independent resistance in 3 minutes $\pm$ 3 seconds.

6.2.1.3 Stress Cycle. The conditions achieved during the pre-cycling stage are repeated continuously (both heating and cooling) until the coupon exceeds one of the rejection criteria or the maximum numbers of cycles has been reached.

6.2.1.4 Graphing. Graphs are automatically generated that depict the performance of all or each coupon under test. Test data can be inputted into various spreadsheet formats for further statistical analysis.

6.2.1.5 Failure Analysis - Optional. Failure site is identified using a multimeter or thermographic system and subsequently microsectioned.

6.2.2 Test Sequence. A description of the equipment sequence is as follows. The sequence described is for an individual coupon, although all installed coupons are processed simultaneously.

6.2.2.1 The auto ranging multimeter measures and displays (on PC monitor) the ambient resistance (voltage drop) of the coupon's inner layer interconnect circuit.

6.2.2.2 The system software calculates and displays the required "target" resistance (temperature). The available stress testing range is from 50°C - 250°C (122°F - 422°F). The equation used to calculate the target resistance is as follows:

$$\text{Target Resistance} = ([\text{TCRI} \times R_{rm} \times T_h] + R_{rm})/1.1$$

where:
TCRI = Thermal coefficient of resistance for the Interconnect
R_{rm} = Resistance of coupon at room temp (25C)
T_h = Specified temperature to be achieved.

6.2.2.3 The system selects and displays a DC current associated to the measured ambient resistance, derived from an internal software library.

NOTE: Additional equations/algorithms used by IST that establish the initial current selection for pre-cycling, relative to the relationship of coupon interconnect resistance TCRI, coupon construction and stress test temperature to be achieved are considered proprietary at this time.

6.2.2.4 The rejection resistance is calculated and displayed. This is adjustable from 1 - 100% increase. If 10% is selected, 10% of the target resistance is calculated and added to the original resistance to establish the rejection criteria.

6.2.2.5 Pre-cycling is initiated by the application of the selected current to the coupon, the computer monitors and records the coupon's performance throughout this first cycle. If at the end of the 1st pre-cycle, the coupon achieves the specified resistance level in 3 minutes $\pm$ 3 seconds, it will be accepted for subsequent stress testing. If the resistance level was not achieved in this time frame, the coupon will automatically be pre-cycled again with a revised/compensated current.

6.2.2.6 Forced air cooling is commenced after each pre-cycle to cool the coupons. (Requires 3.5 minutes)

6.2.2.7 The IST system software will automatically compensate for the difference between what actual resistance was achieved and the target resistance. The system will re-test using revised conditions until all coupons are accepted for stress testing.

NOTE: The equations/algorithms used by IST to compensate the DC current is considered proprietary at this time.

6.2.2.8 The system automatically records and saves all information regarding conditions for subsequent stress testing.

6.2.2.9 The stress test is initiated by re-applying the same DC current level established for each individual coupon during the pre-cycle operation. Three minutes of heating is followed by two to three minutes of cooling. Cooling time is a function of overall thickness and construction of the coupon.

6.2.2.10 Individual coupons are continually recycled using their customized heating and cooling conditions (before failure initiates), until one of the rejection criteria is achieved or the maximum number of cycles is completed.

6.2.2.11 The coupon's resistance "delta" (variance from initial calculated resistance) increases (positively) as failure inception occurs. The rate of change in the delta is indicative of the mechanical change (failure) within the interconnects.

6.2.2.12 When each coupon delta reaches the maximum resistance rejection criteria, IST stress testing is stopped. The rejection criteria prevents thermal runaway (burnout) plus allows for early intervention for failure analysis to be completed effectively.

6.2.2.13 The IST system continuously monitors the two independent circuits of each coupon, recording multiple points of each cycle until the coupon exceeds one of the rejection criteria. The data is compiled to create graphs of each or all coupon's performance throughout IST stress testing. The following are typical graphs generated by good and bad coupons.

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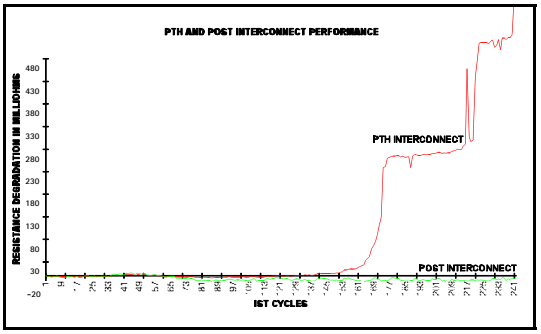
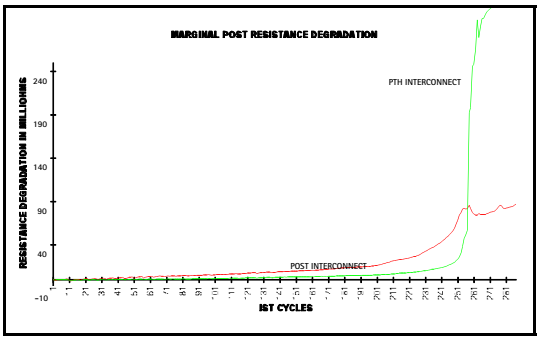
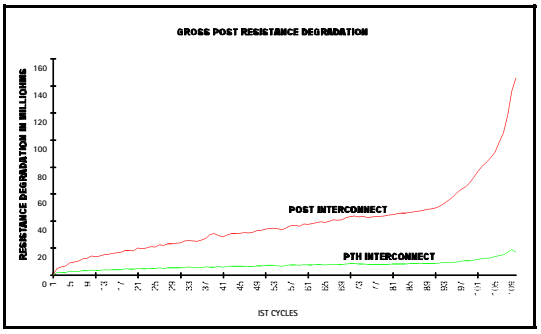
NOTE: The axis are not the same in all three graphs.



This figure shows a plated through hole barrel which begins to fail at 200 cycles while the post remains intact.



This figure shows a post that shows an increase in resistance beginning around 70 cycles while the barrel doesn't completely fail until around 250 cycles.



This figure shows an increase in post resistance at the initial cycle.

6.2.2.14 If rejections are noted, the holes exhibiting the defect can be identified by using a multimeter or thermographic system. These sites can be microsectioned to determine exact location of separations or cracks.

F.8 IPC TM 650: Protocol for Thermal Stress Test for Plated-Through Holes, Number 2.6.8

1. Scope

To standardize the thermal stressing methodology for subsequent evaluation of the copper plating in through holes after exposure to high temperature solder float. The test may be performed on plated-through holes after any stage of plating (e.g., copper, nickel, gold, tin).

2. Applicable Documents

Federal specifications QQ-S-571 and MIL-F-14256, and IPC-TM-650. Test Method 2.1.1.

3. Test Specimen

3.1 Specimen shall be removed from the panel by sawing or equivalent method, 1/4" from the edge of terminal pad area of through holes to be tested.

3.2 Specimens shall be sawed from a printed wiring board or test coupon in such a manner that at least three of the smallest size plated-through holes can be viewed in the finished microsection.

4. Apparatus

4.1 Circulating Air Chamber. Capable of maintaining a uniform temperature of 135°C (275°F) to 149°C (300° F).

4.2 Solder Pot. Electrically heated, thermostatically controlled of sufficient size containing at least 2 pounds of SN63 percent solder conforming to the contaminant level specified in Table II of IPC-S-615.

4.3 Thermocouple indicator. Or other devices to measure the solder temperature 3/4" +/- 1/4" below the surface.

4.4 Desiccator

4.5 Microscope. Range (100x/400x)

4.6 Stop Watch

4.7 Water White Rosin Flux. Type R per MIL-F-14256 or flux agreed upon between customer and vendor.

5. Procedure

5.1 Specimens shall be conditioned by drying in an oven for a minimum of 4 hours at 135°C (275° F) to 149°C (300°F) and cooled to room temperature in a desiccator.

5.2 Remove the specimens from the desiccator using tongs. Flux coat the surface and plated-through holes to ensure solder slugging.

5.3 Remove the dross from the solder pot surface and lay the specimen on the solder maintained at 288° C (550° F) +/-5° C (+/-9° F) for 10 seconds +1. -0 seconds. (The specimens are not to be held against the surface of the molten solder.)

5.4 Using tongs, carefully remove the specimen from the solder and allow to cool to room temperature.

Caution: Do not shock specimens while the solder in the plated-through hole is still liquid.

5.5 Microsection as defined in Test Method 2.1.1 of IPC-TM-650 and examine plated-through holes for degradation of the plated metal or the foil.